Random Demodulator AIC Architecture

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***Abstract*—Compressive Sensing is a sampling paradigm that aims to reconstruct sparse signals (whether in the time or frequency domain) from a reduced number of samples. This form of sampling represents a greater saving of storage, processing and transmission of data, since the amount of information used is reduced. This can be useful in Internet of Things (IoT) applications, for example, which present a scenario of limited resources. Therefore, Analogue-to-Information converters (AIC) are defined as the practical application of the Compressive Sensing theory. In this work, a well-functioning AIC circuit was implemented, using the Random Demodulation architecture.**

***Index Terms*—AIC, Compressive Sensing, Random Demodulator, Analog-to-Information converter**

I. Introduction

Sparsity is the characteristic of some signals, which guarantees that the majority of them will be composed of null or very close to zero components, and that most of their energy will be concentrated in a few components. Thus, it is noticeable that a uniform sampling, where samples are collected at each determined time interval, results in a large number of samples that do not contain relevant information about this signal [1].

Hence, a new sampling paradigm was proposed, Compressive Sensing [2], which allows sparse signals in the time or frequency domain, to be reconstructed from a reduced number of samples. To achieve this, samples are taken at a rate lower than the Nyquist-Shannon rate.

Thus, this form of sampling represents a greater saving of storage, processing and transmission of data, since the amount of information used is reduced. This demonstrates an advantage, when compared to other conventional sampling methods, in Internet of Things (IoT) applications, which present a scenario of limited resources.

Therefore, Analog-to-Information converters (AIC) are defined as the practical application of the Compressive Sensing theory. The main architectures for its implementation are the Random-Modulation Pre-Integrator (RMPI), described in [3], Random Sampling (RS), described in [4], and Random Demodulation (RD).

In this paper the RD architecture was chosen for the implementation of an AIC circuit, taking [5] as a reference.

II. Random Demodulator

The Random Demodulator (RD) architecture is made up of 5 main parts, as shown in Fig. 1, and they are:

a) Analog signal to be processed by the AIC;
b) Input of a sequence of pseudorandom bits;
c) Mixer (analog multiplier);
d) Low-pass filter;
e) Low-rate analog-to-digital converter.

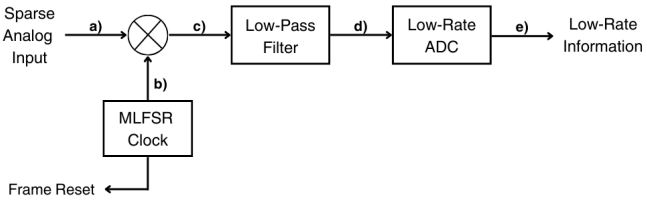

Fig. 1. Random Demodulator (RD) architecture

Initially, the architecture receives a sparse analog input signal, and along with it a sequence of pseudorandom bits is received. These bits are obtained through an MLFSR Clock (Maximum-Length Linear Feedback Shift Register). After this, the two input signals pass through an analog multiplier, where they will be mixed, in order to modulate the analog input signal with a +-1 sequence, and their output must be proportional to the product between the two inputs. After leaving the mixer, the signal passes through a low-pass filter, to reduce the noise, allowing only low-frequency signals to pass through it, and attenuating high-frequency signals. Finally, the resulting signal is received by a low-rate analog-to-digital converter to be quantized.

It is possible to observe the changes that the signal undergoes in Fig. 2, where a) and b) show a sine wave and the MLFSR, respectively, c) displays the waveform of the two input signals mixed, and d) shows the waveform after the low-pass filter.

III. Related Works

Recently, research has demonstrated that AIC is successful in guaranteeing signal reconstruction, from a fewer number of samples, for sparse signals [6]. In [7], it was demonstrated that the random demodulation AIC can compress and reconstruct sinusoidal, multisine and ECG signals, when using subsampling.

For the signal reconstruction stage, it is necessary to use reconstruction algorithms, such as Orthogonal Matching Pursuit (OMP), Compressive Sampling Matching Pursuit (CoSaMP) and CVX. In [8] CoSamp performs better than OMP, when

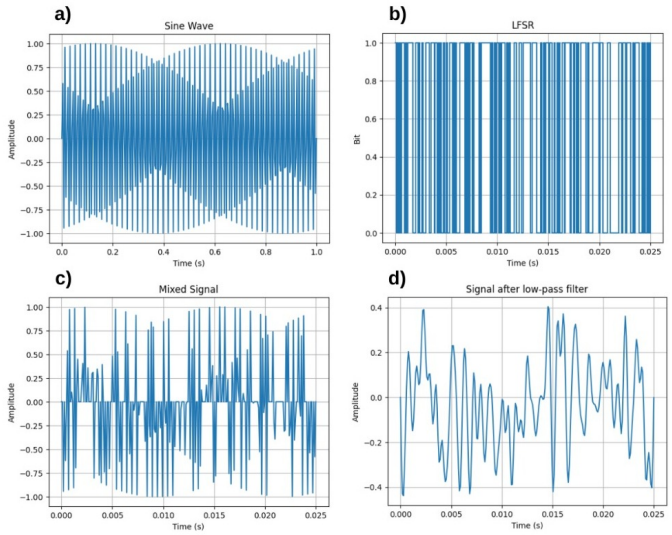

Fig. 2. Signal display at each AIC step: a) Analog sparse signal input b) Pseudorandom sequence of bits input; c) Mixer output; d) Low-pass filter output

comparing their average squared error. However, from what is shown in [9], OMP can find more correct frequency components than CoSaMP, and CVX obtains lower Mean Square Error (MSE) values.

Thus, promising results are expected, since other implementations of the same architecture have already shown good results, as seen in [6]–[9].

IV. Architecture Implementation

The construction of the MLFSR was done using Quartus II, and a DE0-NANO model FPGA, implemented in the System-Verilog language. Initially, a 4-bit shift register and a clock divider (slow clock) based on a counter are created, which reduces the original FPGA clock frequency from 50 MHz to 10 kHz. After this, an "XOR" gate receives the outputs of the third and fourth registers, serving as input to the first register, which generates a change in its state and consequently, in the state of the others, at each beat of the slow clock. This generates the change of states and, consequently, the pseudorandomness of the sequence, which can be seen in Fig. 3.

For the hardware implementation, the mixer and the low-rate ADC devices were purchased as bench components, and their models are, respectively: AD633 JR (Analog Devices Inc.) and ADS1115 (Texas Instruments). The low-pass filters were made by combining a 1k Ohm resistor with a 100nF ceramic capacitor, to obtain a cutoff frequency of approximately 1.6 kHz, and a 10k Ohm resistor with a 100nF ceramic capacitor, to obtain a cutoff frequency of approximately 160 Hz.

For the laboratory tests, we employed the following tools and equipment: Oscilloscope model DSO-2150 USB (Hantek), Signal generator model POL-40 (Politerm), and an HF-3205D source (Politerm). The setup with the equipment used in the laboratory tests is shown in Fig. 4.

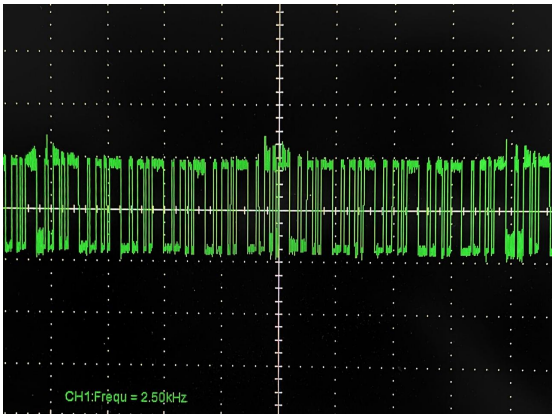

Fig. 3. 10kHz MLFSR displayed on the oscilloscope

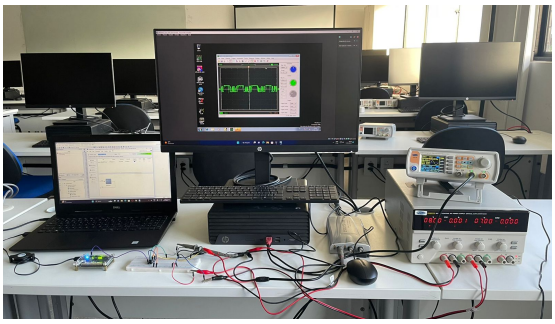

Fig. 4. Setup used in laboratory tests

For the circuit testing, a 100 Hz sine wave was generated in the signal generator, and together with the FPGA's 10 kHz MLFSR, it was processed by the mixer, through a breadboard. After that, the output signal passed through a common RC low-pass filter, and its cutoff frequency was adjusted throughout the tests. Finally, the oscilloscope was used to read the desired signals.

In Fig. 5 it can be seen the mixer´s output, i.e., the result of the modulation between the input sparse signal and the

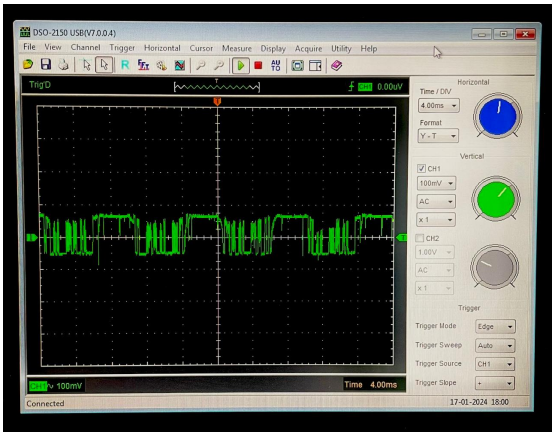

Fig. 5. Mixer output displayed on the oscilloscope, which input signals are a sine wave of 100Hz and the MLFSR of 10kHz

MLFSR.

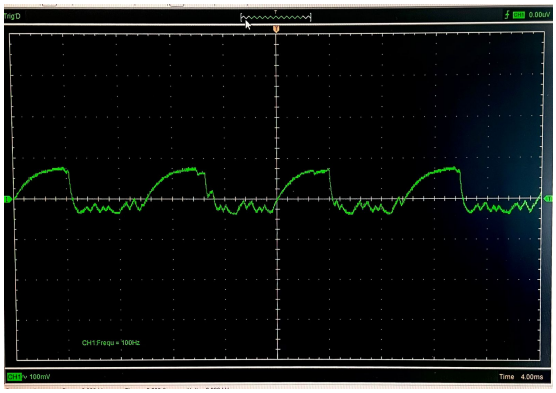

Fig. 6. RC low-pass filter output with cutoff frequency of 160Hz

The Figs. 6 and 7 show the result at the integrator output, implemented through the low-pass filter, with cutoff frequencies of 160Hz and 1.6kHz, respectively. The output is the integration of the multiplication of the sine wave of 100Hz with an amplitude of 5V, and the pseudo-random sequence of +-1 with a frequency of 10kHz.

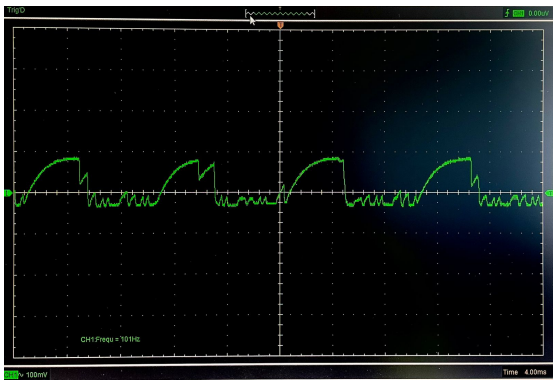

Fig. 7. RC low-pass filter output with cutoff frequency of 1.6kHz

V. Conclusions

In this paper, an experimental evaluation of AIC Random Demodulation architecture was made. The implementation was carried out using a pseudorandom sequence generator (MLFSR) implemented in SystemVerilog. The chosen input signal was a one-tone sinusoid, considered sparse in the frequency domain. The architecture was implemented with off-the-shelf components (FPGA De0, integrated circuit of a multiplier, AD633).

In future work, it is possible to test the sampling of other sparse signals, such as the cardiac signal, as well as evaluating the reconstruction of signals with optimization algorithms such as OMP and CVX.

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